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09/438,288	11/12/1999	CHENGKE SHENG	SC91189A	9114

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HARRY A WOLIN
MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY LAW SECTION
7700 WEST PARMER LANE MD TX32 PL02
AUSTIN, TX 78729

EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 01/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,288	SHENG, CHENGKE	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. DETAILED ACTION

2. Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. Claim Objections

5. Claim 16 objected to because of the following informalities: There should be an "an" instead of "a" before the word incrementer. Appropriate correction is required.

6. Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

8. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1 and 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 recites the limitation "the first accumulator". There is insufficient antecedent basis for this limitation in the claim.

11. Claim 16 is indefinite since it has further comprising without noting a claim number.

12. Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

14. A person shall be entitled to a patent unless –

15. (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Murai USPN 6154487.

17. As per claim 4, Murai teaches a chip rate base band processor which receives digital information containing symbol information and provides a symbol output, comprising:

18. an input memory which stores the digital information (Murai fig. 2: inherent for the RX baseband signal to be stored);

19. a pilot correlator having an input coupled to the input memory, and an output (Murai fig. 2: 201);

20. a data correlator having an input coupled to the input memory, and an output (Murai fig. 2: 202);

21. a pilot memory coupled to the pilot correlator (Murai fig. 2: 206 delay is a type of memory);

22. a channel estimator having an input coupled to the pilot memory, and an output (Murai fig. 5: 226);

23. a data memory having an input coupled to the data correlator (Murai fig. 2: 212 has a selector and thus it is storing data which makes it a memory (212 is inside a high accuracy acquiring means));

24. a phase rotator (Murai fig. 10: 112A) having a first input coupled to the output of the channel estimator (Murai fig. 5: 226; combination of figures 5 and 10), a second input coupled to the data memory (Murai fig. 10: 112A has an input coupled to a high accuracy acquiring means which fig. 2 shows has a selector and thus it is storing data which makes it a memory), and an output (Murai fig. 10: output of 112A); and

25. a symbol combiner having an input coupled to the output of the phase rotator, and an output which provides the symbol output (Murai fig. 31: 107; paragraph 63: "Though it is not shown in FIG. 10, the output result is sent to the symbol combiner 107 of FIG. 31.").

26. Claims 7-11 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Okamoto et al. USPN 5960028.

27. As per claim 7, Okamoto teaches in a chip rate base band processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of:

28. storing the digital information (Okamoto fig. 5: 5);

29. multiplying a PN code (Okamoto fig. 5: 7) with a first segment (Okamoto fig. 5: P1, D1, 11), representative of the predetermined time duration (Okamoto fig. 5: Serial data has been divided into 4 sets of parallel data P1 to P4 and thus there are different time durations for each), of the stored digital information and multiplying the PN code (Okamoto fig. 5: 7) with a second segment (Okamoto fig. 5: P2, D2, 13), representative of the predetermined time duration

(Okamoto fig. 5: Serial data has been divided into 4 sets of parallel data P1 to P4 and thus there are different time durations for each), of the stored digital information.

30. As per claim 8, Okamoto teaches in a chip rate base band processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of: storing the digital information; and successively multiplying a first PN code (Okamoto fig. 5: B1) with a first plurality of segments of the stored digital information (Okamoto fig. 5: multiple data in D1 and thus we obtain multiple plurality of segments), wherein each segment is representative of the predetermined time duration (Okamoto fig. 5: Serial data has been divided into 4 sets of parallel data P1 to P4 and thus there are different time durations for each).

31. As per claim 9, Okamoto teaches the method of claim 8 further comprising successively multiplying a pilot PN code with the first plurality of segments of the stored digital information (Okamoto fig. 5: 7, delays, modulators).

32. As per claim 10, Okamoto teaches the method of claim 8, wherein the first PN code is a data code (Okamoto paragraph 312 "Referring to FIG. 30, when signals a2 and a3 are to be differentiated, control of the window (period T.sub.M of FIG. 30) and maintaining of integration of PDI are performed by using the signal a1 (preceding the signal a2 by one delay time), which precedes signals a2 and a3, as a pilot signal."; paragraph 325 "In summary, in the present

embodiment, two or more signals earlier in time are used as pilot signals, ... "; Thus, the data and pilot codes are being interchanged).

33. As per claim 11, Okamoto teaches the method of claim 8, wherein the first PN code is a pilot code (Okamoto paragraph 312 "Referring to FIG. 30, when signals a2 and a3 are to be differentiated, control of the window (period T.sub.M of FIG. 30) and maintaining of integration of PDI are performed by using the signal a1 (preceding the signal a2 by one delay time), which precedes signals a2 and a3, as a pilot signal."; paragraph 325 "In summary, in the present embodiment, two or more signals earlier in time are used as pilot signals, ... "; Thus, the data and pilot codes are being interchanged).

34. As per claim 15, Okamoto teaches a chip rate base band processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of a memory which stores digital information representative of a plurality of the predetermined time durations; a first multiplier coupled to the memory; and a first PN code buffer coupled to the first multiplier (Okamoto discussed above).

35. As per claim 16, Okamoto teaches the chip rate base band processor further comprising a incrementer means for to successively outputting a portion of the digital information from the memory to the multiplier in segments (Okamoto fig. 5: data has been divided into parallel segments) representative of the predetermined time duration (remainder discussed above).

36. As per claim 17, Okamoto teaches the chip rate base band processor of claim 16 further comprising: a second multiplier coupled to the memory; and a second PN code buffer coupled to the second multiplier (Okamoto discussed above).

37. Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

39. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murai.

41. As per claim 5, Murai teaches the chip rate base band processor of claim 4 further comprising a second data correlator coupled to the input memory (Murai teaches a data correlator in fig. 2 with element 202. What Murai does not teach is a second data correlator. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the data correlator, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.).

42. As per claim 6, Murai teaches the chip rate base band processor of claim 5 further comprising: a second data memory coupled to the second data correlator; a second phase rotator having a first input coupled to the output of the channel estimator, a second input coupled to the

second data memory, and an output; and a second symbol combiner having an input coupled to the output of the phase rotator, and an output which provides the symbol output. (What Murai shows are singular elements of this claim. Murai does not double these elements. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the elements, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.)

43. Claims 12, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto.

44. As per claim 12, Okamoto teaches the method of claim 8, further comprising multiplying a second PN code (Okamoto shows 1 PN code. Okamoto does not show a second PN code. It would have been obvious to one having ordinary skill in the art at the time the invention was made to show a second PN code, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.) with a second plurality of segments of the stored digital information (Okamoto fig. 5: P2, D2, 13), wherein each segment is representative of the predetermined time duration (Okamoto fig. 5: Serial data has been divided into 4 sets of parallel data P1 to P4 and thus there are different time durations for each).

45. As per claim 13, Okamoto teaches the method of claim 12, wherein the first PN code and the second PN code are data PN codes (Okamoto paragraph 312 "Referring to FIG. 30, when signals a2 and a3 are to be differentiated, control of the window (period T.sub.M of FIG. 30) and maintaining of integration of PDI are performed by using the signal a1 (preceding the signal a2 by one delay time), which precedes signals a2 and a3, as a pilot signal."; paragraph 325 "In

summary, in the present embodiment, two or more signals earlier in time are used as pilot signals, ... "; Thus, the data and pilot codes are being interchanged).

46. As per claim 14, Okamoto teaches the method of claim 13 further comprising: successively multiplying a first pilot PN code with the first plurality of segments of the stored digital information; and successively multiplying a second pilot PN code with the second plurality of segments of the stored digital information (Okamoto discussed above).

47. Allowable Subject Matter

48. Claims 1, 2 and 3 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

49. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the underlined portion:

50. As per claim 1, Murai teaches a chip rate base band processor which receives digital information containing symbol information and provides a symbol output, comprising:

51. an input memory which stores the digital information (Murai fig. 2: inherent for the RX baseband signal to be stored);

52. a data PN code buffer (Murai fig. 2: 204);

53. a pilot PN code buffer (Murai fig. 2: 204 with 205);

54. to a pilot multiplier having a first input coupled to the pilot PN code buffer, a second input coupled to the input memory, and an output (Murai fig. 2: multiplier in 202);

55. a data multiplier having a first input coupled to the data PN code buffer, a second input coupled to the input memory, and an output (Murai fig. 2: multiplier in 201);

56. a pilot accumulator having an input coupled to the output of the first multiplier, and an output (Murai fig. 2: integration inside 202);

57. a pilot memory coupled to the first accumulator (rejected with 112; Murai fig. 2: selector inside 212 is inherently a memory);

58. a channel estimator coupled to the pilot memory (Murai fig. 5: 226);

59. ***a peak detector coupled to the pilot memory (not in Murai)***;

60. a data accumulator coupled to the data multiplier;

61. load controller having a first input coupled to the peak detector, a second input coupled to data accumulator, and an output;

62. a data memory coupled to the load controller;

63. a phase rotator having a first input coupled to the channel estimator, a second input coupled to the data memory, and an output; and

64. a symbol combiner having an input coupled to the phase rotator, and an output which provides the symbol output.

65. Claims 2 and 3 depend on claim 1.

66. Conclusion

67. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gilhousen et al USPN 5103459.

68. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

69. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

70. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

71. 72.

73. PK
74. January 7, 2003

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 1/8/03